GaAs HBT PIN Diode Attenuators and Switches

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ABSTRACT

We report on an AlGaAs/GaAs HBT 2-stage pin diode attenuator from 1-10 GHz and an X-band 1-pole 2-throw X-band pin diode switch. The 2-stage pin attenuator has over 50 dB dynamic range at 2 GHz and a maximum IP3 of 9 dBm. The minimum insertion loss is 1.7 dB per stage and has a flat response to 10 GHz. The X-band switch has an insertion loss of 0.82 dB and an off-isolation of 25 dB. The bandwidth is greater than 35 % and the IP3 is greater than 34.5 dBm. Both of these circuits consists of PIN diodes constructed from the base-collector MBE layers of our base-line HBT process. This work demonstrates the monolithic integration of pin diode switch and attenuation functions in an HBT technology without additional process or MBE material growth.

Introduction

Pin diodes are used in many microwave communication systems because of their high breakdown voltages, fast switching characteristics, and their variable resistance characteristics with bias. They provide circuit functions in broadband switches, attenuators, photo-detectors, and variable gain amplifiers. Most uses of pin diodes have been as discrete components integrated in a hybrid circuit. This makes it cumbersome for the designer because it involves a lot of bench testing/tuning to make the circuit work correctly.

In GaAs HBT technology, the pin diode can be constructed from existing material layers, allowing the monolithic integration of pin diodes with HBT transistors. The lightly doped collector layer of the HBT device structure can be used as the intrinsic layer of the pin. The heavily doped base and sub-collector act as the P^+ and N^+ type material. With no modification to the existing baseline HBT process, reasonable pin attenuator and switching performance was achieved. Because the HBT and pin diode structures are compatible, HBT technology offers additional circuit functionality at no added expense. This makes it attractive for commercial applications where cost is a major factor. For military applications where peformance of both HBT and pin diodes are of major concern, an optimized pin structure can be separately grown using selective MBE techniques, but at the expense of a more complex process.

This paper presents the performance of an HBT pin attenuator and an X-band 1-pole 2-throw switch made from the the intrinsic device layers of our baseline HBT process.

GaAs HBT Process Technology

The MBE profile of our standard GaAs HBT process is shown in fig. 1. This profile incorporates a base thickness of 1400Å uniformly doped to $1x10^{19}$ cm^{-3}, a collector thickness of 7000Å lightly doped N-type of $7x10^{15}$ cm^{-3},

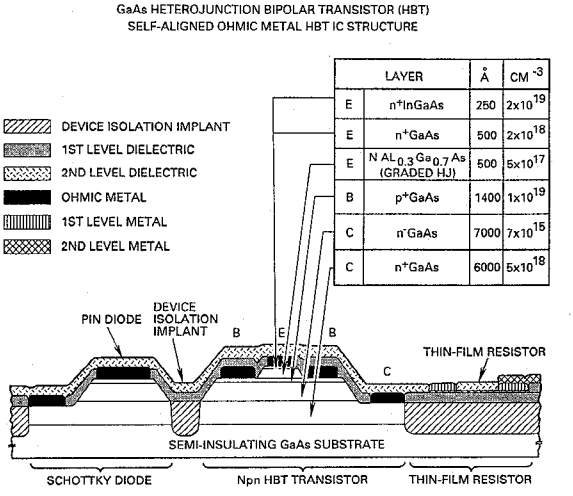

Fig. 1 HBT PIN diode MBE profile.

and an N^+ subcollector doped to $5x10^{18}$ cm^{-3}. The lightly doped collector is used to contruct the intrinsic layer of the pin diode. The heavily doped base and sub-collector constructs the P^+ and N^+ type layers of the pin. The reverse breakdown voltage is greater than 20 volts. The reverse bias capacitance per square micron of the pin is 0.162 $fF/\mu m^2$ at full depletion, however, this does not include the lateral parasitic capacitances which are about twice the parallel diode depletion capacitance. The series on-resistance of the diode is 600 Ω-μm^2 and is mainly due to the ohmic contact resistance of the base and collector. The baseline HBT transistors have an f_t and f_{max} of 24 GHz and 38 GHz, respectively. This baseline process consists of a 2 μm emitter Self-aligned Base Ohmic Metal HBT (SABM) technology which incorporates nichrome 100 Ω/square TFR's, MIM capacitors, schottky diodes, spiral inductors, back-side vias, as well as the pin diodes.

PIN diode Model

The performance of the pin diode is dependent on several factors involving the MBE layers. These layers are both used in the HBT transistor and the pin diode. The advantages of the HBT device structure for the pin diode is that the HBT device base is usually doped deep into degeneracy in order to achieved low lateral and ohmic contact base resistance. This improves the f_{max} of the HBT devices. It also improves the on-resistance of the pin diode. The wide and very lightly doped collector gives the pin diode a low series off-capacitance, however, small-signal modelling indicates that about 60 % of this capacitance is influenced by the

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parasitic sidewall capacitances. This is because the pin diode layout for these circuits were interdigitated like the HBT device emitter fingers instead of a conventional round diode structure. The geometrically round type of layout will reduce the parasitic capacitances and improve the performance. In addition to reducing the capacitance, a wider collector will increase the breakdown voltage, however, this will degrade the f_t performance of the HBT device. Thus, optimization of both HBT device and pin diode MBE layers depends on the performance requirements of the circuit application. In this paper, we report the pin diode circuit performance of our base-line HBT process.

A pin diode model was derived using both dc and small-signal s-parameters. A typical I-V curve of a 5 x 15 μm^2 dual base finger pin diode is shown in fig. 2. The ideality factor of the HBT pin diode was found to be about 2.03. The small-signal modelling was done over the forward bias region and a forward bias model was derived. The reverse bias model was obtained by small-signal extraction of the reverse bias capacitance at zero bias. Since calculations show that the pin diode is almost fully depleted at zero bias, about 5/7 depleted, the zero bias capacitance was used with the assumption of a 35 % reduction in value for full reverse bias depletion. Fig. 3 shows the forward and reverse bias model of

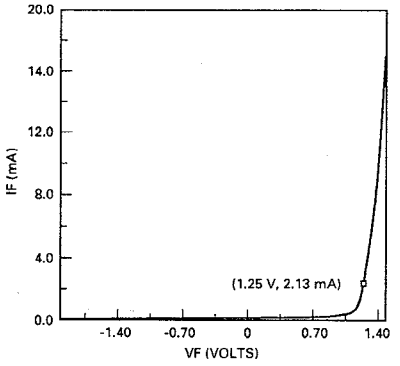
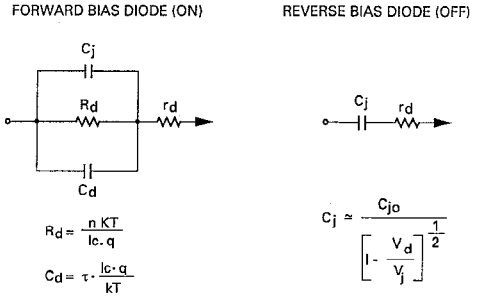


Fig. 2 HBT PIN dc I-V characteristics.



MODEL PARAMETER	SYMBOL	VALUE
SERIES CONTACT RESISTANCE	r_d	3.5-4Ω
ZERO BIAS DEPLETION JUNCTION CAPACITANCE	C_{jo}	0.097 pF
JUNCTION POTENTIAL	V_j	0.356V
GRADING COEFFICIENT	M	0.5
IDEALITY FACTOR	n	2.03
SATURATION CURRENT	I_s	6.58×10^{-14}A
REVERSE BREAKDOWN VOLTAGE	V_{BR}	>20V
TRANSIT TIME	τ	0.21 ps

Fig. 3 HBT PIN diode model.

a 5 x 15 μm^2 dual base finger pin diode. In the forward bias operation, the dynamic resistance is a function of current given by $G_m = I_c{*}q/(n * kT)$, where n is the ideality factor. The parallel diffusion capacitance is approximately given by $C_d = T_{au} * G_m$. T_{au} was imperically extracted from the small-signal modelling over bias current. The series ohmic contact resistance r_d was also obtained from small-signal modelling. This model was used for both the attenuator and the SPDT X-band switch.

PIN diode Attenuator

The schematic of the 2-stage pin diode attenuator is shown in fig. 4. The single stage pin diode attenuator circuit consists of a series and a shunt diode to form a T-network. The T-network was used in order to obtain a combination of good insertion loss and attenuation range. The low frequency response is limited by the 15 pF blocking capacitors. In this design the series and shunt diodes are biased through a range of forward biases. The diodes are never fully reverse biased. A fixed supply of 12 Volts and a variable attenuation voltage ranging from 0 to 12 Volts was used. A maximum current of 6 mA was measured for the diodes in the forward bias state for each stage. A photograph of the 2-stage pin diode attenuator circuit is shown in fig. 5. This chip measures 1.2 x 1.8 mm^2.

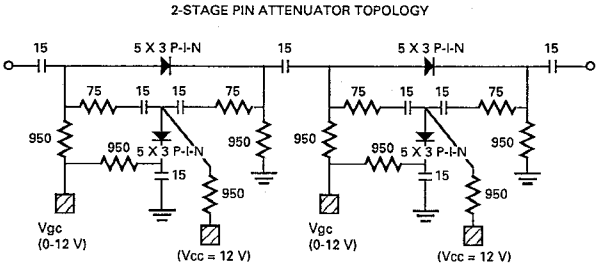


Fig. 4 Schematic of the 2-stage HBT PIN diode attenuator.

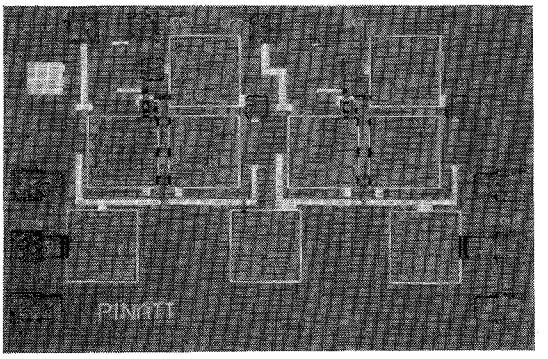


Fig. 5 Photograph of the HBT PIN diode attenuator chip. Chip size is 1.2 x 1.8 mm^2.

The variable attenuation performance from 0.05 to 10 GHz is shown in fig. 6. The minimum insertion loss is 3.4 dB for two stages. The graph shows insertion loss response over the full band for ≈ 5 dB steps @ 2 GHz. The insertion loss flatness becomes compromised at the higher attenuation states because the shunt and series diodes are under forward bias where the diffusion capacitance shunts the dynamic resistance at higher frequencies. This gives the positive slope in the response. The low end cut-off is due to the size of the blocking capacitors used. The low end response could be extended by incorporating larger off-chip capacitors. Fig. 7 shows the return loss performance over the attenuation range. The input

and output return-losses are maintained at about 10 dB and are fairly insensitive over the attenuation range. Fig. 8 shows modelled vs. measured insertion-loss as a function of voltage, V_{gc}, @ 2 GHz. The general voltage control characteristics agree over the attenuation range. The dynamic range at 2 GHz is greater than 50 dB. IP3 of about 9 dBm was measured from 2-4 GHz at minimum insertion loss. The low IP3 is mainly due to the soft forward bias of the on-series diodes and the lack of full reverse bias of the off-shunt diodes. By further forward biasing the series diodes and reverse biasing the shunt diodes, the IP3 was improved by about 5 dBm. At the higher attenuation states the IP3 degrades more because both shunt and series diodes are softly forward biased. The biasing scheme could be re-designed in order to obtain higher IP3 at the expense of more power consumption.

X-band 1-Pole 2-Throw Switch

Pin diodes are used as switches because of their compact size, high frequency and power handling capability. They are often used in transceiver systems where high frequency and power are main performance drivers. For this reason, the monolithic integration of pin diodes can be very useful in HBT technology.

A SPDT X-band pin diode switch was developed to demonstrate the ability to integrate pin diode switch functions in an existing HBT technology. A circuit schematic of a Single-Pole Two-Throw microwave switch is shown in fig. 9. Each arm of the switch consists of two 5x15 μm^2 dual base shunt pin diodes. The shunt configuration has the advantage of reliable thermal performance (lower thermal resistance). Quarter-wavelength lines transform the low impedance "on"-diode to an open at the output port for good isolation. Quarter-wave transformers are also used as rf chokes in the bias network of each pin diode arm. MIM capacitors were used to terminate the quarter-wave lines instead of radial stubs in order to suppress coupling which could degrade the off-isolation. A photograph of the pin diode X-band switch is shown in fig. 10. The chip area is 2.4 x 2.4 mm^2. A plot of the insertion loss and isolation is shown in fig. 11. The insertion loss is 0.82 dB at 10 GHz. The 1-dB bandwidth of the insertion loss is around 35 % and is limited by the bandwidth of the quarter-wave transformers. The "off" isolation is about 25 dB. This is less than expected (≈ 35 dB) and simulations show that this is probably due to a higher than expected ohmic contact resistance. The input and ouput return losses at 10 GHz are better than 15 dB and are shown in fig. 12. The IP3 was found to be very dependent on the reverse bias of the pin diode in the "on" arm. The IP3 was measured for various reverse bias voltages of the shunt pin diode. Fig. 13 illustrates that for greater reverse biases, the IP3 improves. At a reverse bias of 7 volts the IP3 was +34.5 dBm. The IP3 was not measured for higher reverse biases because of the limitations of our measurement system (35 dBm). The reverse bias breakdown is around 20 Volts for these pin diodes.

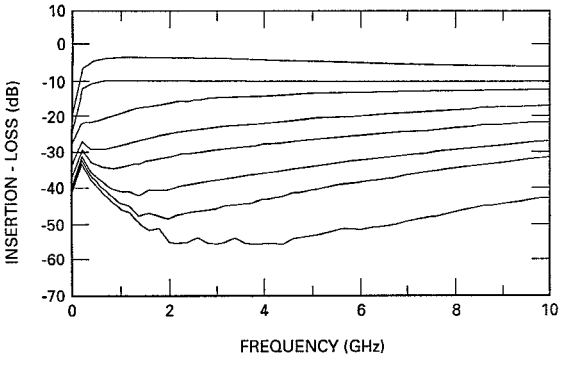


Fig. 6 Variable attenuation performance from 0.05-10 GHz.

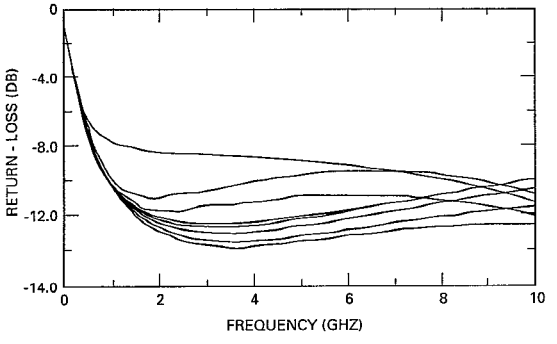


Fig. 7 Return-loss over the attenuation range.

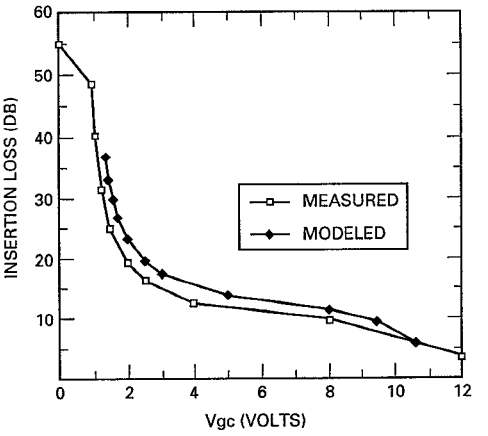


Fig. 8 Measured and modelled insertion-loss as a function of voltage control at 2 GHz.

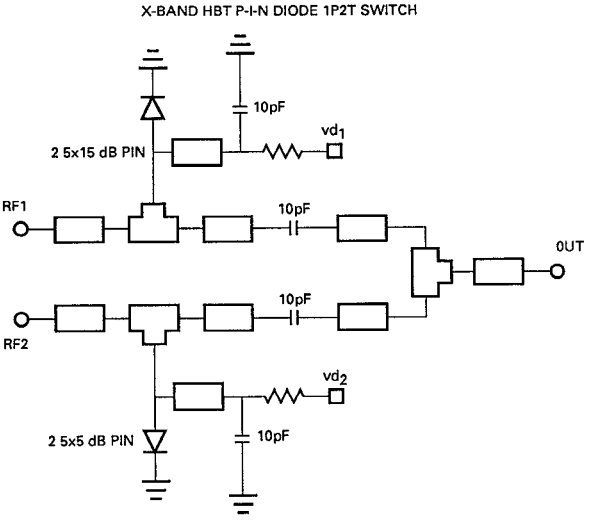


Fig. 9 Schematic of the 1P2T X-band PIN diode switch.

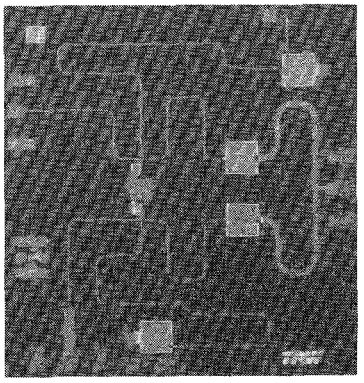


Fig. 10 Photograph of the 1P2T X-band PIN diode switch. Chip size is 2.4 x 2.4 mm^2.

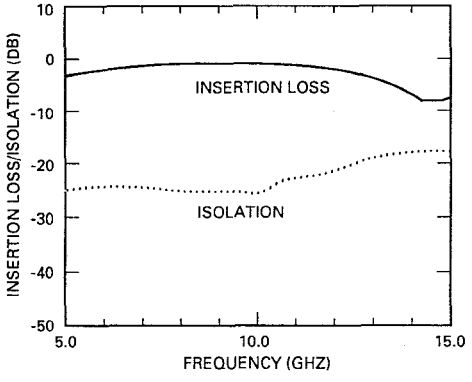


Fig. 11 Insertion loss and off-isolation performance of the X-band switch.

Conclusion

Pin diode attenuation and switching functions were demonstrated using a Self-aligned Base Ohmic Metal AlGaAs/GaAs HBT technology. A 2-stage pin diode attenuator from 1-10 GHz was demonstrated with a minimum insertion loss of 3.7 dB, an attenuation range greater than 45 dB, and a maximum IP3 of 9 dBm. An X-band 1P2T switch was also demonstrated with a minimum insertion loss of 0.82 dB, greater than 35% bandwidth, an off-isolation of 25 dB, and an IP3 of at least 34.5 dBm. The pin diodes were constructed from exitsting MBE layers of TRW's base-line HBT process with no additional optimization of the process or material growth.

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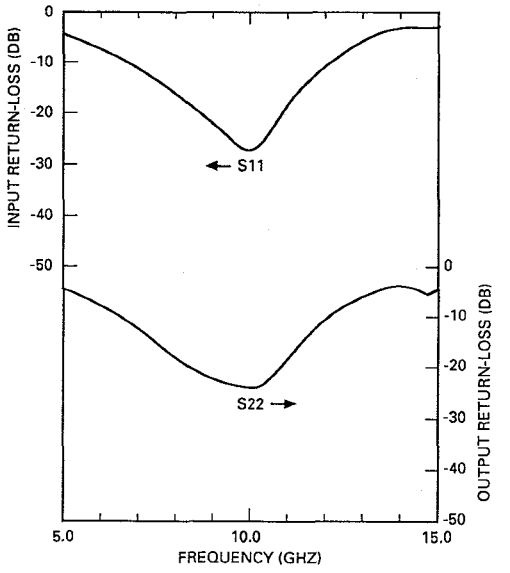

Fig. 12 Input and output return-loss performance of the X-band switch.

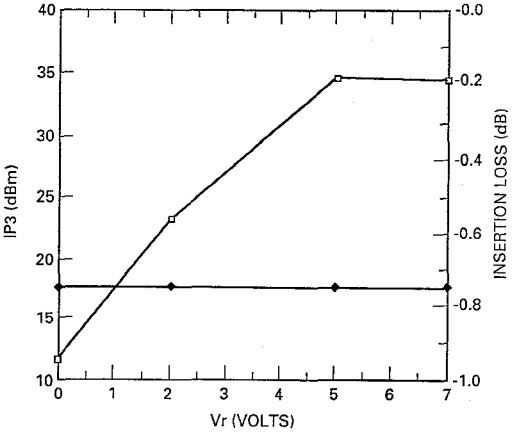

Fig. 13 IP3 performance at 10 GHz as a function of PIN diode reverse bias of the "on" arm.

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